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Shunpei YAMAZAKI)
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For: NONVOLATILE MEMORY AND ELECTRONIC APPARATUS)

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Sir:

I, Mika TATSUMI, C/O Semiconductor Energy Laboratory Co., Ltd. 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan, a translator, herewith declare:

that I am well acquainted with both the Japanese and English Languages;

that I am the translator of the attached English translation of the Japanese Patent Application No. 09-340754 filed on November 26, 1997; and

that to the best of my knowledge and belief the following is a true and correct English translation of the Japanese Patent Application No. 09-340754 filed on November 26, 1997.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 7th day of June, 2006

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[Title of the Invention] NONVOLATILE MEMORY AND ELECTRONIC APPARATUS

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[List of Attachment]

[Attachment] Specification 1

[Attachment] Drawing 1

[Attachment] Abstract 1

[Name of Document] Specification

[Title of the Invention] NONVOLATILE MEMORY AND ELECTRONIC APPARATUS

[Scope of Claims]

[Claim 1]

A nonvolatile memory characterized by including:

over a substrate having an insulating surface,

a source region, a drain region, and an active region formed using a semiconductor thin film which is a single crystal or is regarded as substantially single crystal;

impurity regions provided locally in the active region; and

an intrinsic or a substantially intrinsic channel forming region interposed between the impurity regions.

[Claim 2]

A nonvolatile memory characterized by including:

over a substrate having an insulating surface,

a source region, a drain region, and an active region formed using a semiconductor thin film which is a single crystal or is regarded as substantially single crystal;

impurity regions provided locally in the active region; and an intrinsic or a substantially intrinsic channel forming region interposed between the impurity regions,

wherein said impurity regions comprise an element selected from group 13 or group 15.

[Claim 3]

A nonvolatile memory characterized by including:

over a substrate having an insulating surface,

a source region, a drain region, and an active region formed using a semiconductor thin film which is a single crystal or is regarded as substantially single crystal;

impurity regions provided locally in the active region; and an intrinsic or a substantially intrinsic channel forming region interposed between the impurity regions,

wherein said impurity regions comprise an element selected from group 13 or group 15, and said impurity regions prevent a depletion layer from expanding from the drain region toward the source region.

[Claim 4]

A nonvolatile memory according to claims 1 to 3, wherein the impurity regions are formed from the source region to the drain region in a stripe shape.

[Claim 5]

A nonvolatile memory according to claims 1 to 4, wherein a concentration of the element included in the impurity regions is 1×10^{17} to 5×10^{20} atoms/cm^3.

[Claim 6]

A nonvolatile memory according to claims 1 to 5, wherein the substrate having an insulating surface is a crystallized glass provided with an insulating film on a surface thereof.

[Claim 7]

An electronic apparatus utilizing the nonvolatile memory according to claims 1 to 6 as a recording medium.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention pertains]

The present invention relates to an SOI configuration of a nonvolatile memory formed by using a semiconductor thin film which is single crystal or is regarded as to be substantially single crystalline. In particular, the invention is effective for a nonvolatile memory in which the channel length is 2 μ or less or even 0.5 μ or less.

[0002]

[Conventional Art]

The IC memories that perform data storage and holding in computers are generally classified into the RAM and the ROM. As examples of the RAM (random access memory), the DRAM (dynamic RAM) and the SRAM (static RAM) are given. If the power is turned off, data stored in the DRAM or the SRAM are lost.

[0003]

On the other hand, as examples of the ROM (read-only memory), the mask ROM and the PROM (programmable ROM) are known. The mask ROM and the PROM have an advantage that even if the power is turned off, data stored there are not lost. The PROM is classified into the EPROM (erasable-PROM) in which data erasure is performed by using ultraviolet light, the EEPROM (electrically-EPROM) in which data erasure is performed electrically, the flash memory (flash-EEPROM) in which data erasure is performed en bloc electrically, etc.

[0004]

To fully utilize their marked advantage of permanent data holding, studies and developments on nonvolatile memories have been made energetically. At present, the possibility of a substitute for magnetic memories is being discussed.

[0005]

As for such IC memories, it is necessary to not only improve the reliability and performance but also increase the storage capacity. That is, as in the case of other types of ICs, they are being developed according to the scaling law while miniaturization techniques are always adopted.

[0006]

However, since basically nonvolatile memories store data with use of the same principle of operation as field-effect transistors (hereinafter referred to as FETs), the short channel effect, which is known as causing serious problems in the FET operation as the miniaturization advances, also causes serious problems in the operation of nonvolatile memories.

[0007]

In particular, the phenomenon called punch-through decreases the source-drain voltage and hence makes the current control with the gate electrode difficult. Conventionally, there is an devised example of a bocket structure for increasing the punch-through resistance, for example.

[0008]

[Problems to be Solved by the Invention]

The above-described pocket structure is a structure in which an impurity region having the same conductivity type as the substrate is provided in the channel/drain junction portion. This structure can prevent the occurrence of a punch-through phenomenon by suppressing the expansion of the drain depletion layer.

[0009]

However, in nonvolatile memories, electron-hole pairs are generated by positively causing impact ionization in the channel/drain junction portion. Therefore, a large amount of holes flow to the substrate side at the same time when electrons are injected into the floating gate.

[0010]

On the contrary, in the above-described pocket structure, a large amount of generated holes are stored under a channel forming region. As a result, a phenomenon called a substrate floating effect is generated. This state may cause a problem that the quantity of electric charges which move in the channel forming region cannot be controlled in a control gate.

[0011]

The present invention has been made in view of the above problems, and an object of the invention is therefore to realize a high-performance memory by effectively preventing or weakening the short channel effect that occurs in miniaturizing nonvolatile memories.

[0012]

[Means for Solving the Problem]

A structure of the invention disclosed in this specification is characterized in that a nonvolatile memory comprising: over a substrate having an insulating surface, a source region, a drain region, and an active region formed using a semiconductor thin film which is a single crystal or is regarded as substantially single crystal; striped form impurity regions provided in the active region; and an intrinsic or a substantially intrinsic channel forming region interposed between the impurity regions.

[0013]

In addition, another structure of the invention is characterized in that a nonvolatile memory comprising: over a substrate having an insulating surface, a source region, a drain region, and an active region formed using a semiconductor thin film which is a single crystal or is regarded as substantially single crystal; striped form impurity regions provided in the active region; and an intrinsic or a substantially intrinsic channel forming region interposed between the impurity regions, wherein said impurity regions comprise an element selected from group 13 or group 15.

[0014]

In addition, another structure of the invention is characterized in that a nonvolatile memory comprising: over a substrate having an insulating surface, a source region, a drain region, and an active region formed using a semiconductor thin film which is a single crystal or is regarded as substantially single crystal; striped form impurity regions provided in the active region; and an intrinsic or a substantially intrinsic channel forming region interposed between the impurity regions, wherein said impurity regions comprise an element selected from group 13 or group 15, and said impurity regions prevent a depletion layer from expanding from the drain region toward the source region.

[0015]

In the above structure, it is preferable that the impurity regions be provided in striped form from the source region to the drain region.

[0016]

In the above structure, it is preferable that an element contained in the impurity regions have a concentration that is 1×10^{17} to 5×10^{20} atoms/cm^3.

[0017]

In addition, it is effective to form a memory circuit using a nonvolatile memory having the above structure as a recording medium, and to incorporate it into an electronic apparatus.

[0018]

The main feature of the invention is that impurity regions are formed locally in the active region and the impurity regions prevent a depletion layer from expanding from the drain region toward the source region. In this specification, a region that is enclosed by a source region, a drain region, and field oxide films is called an active region and the active region is divided into impurity regions formed locally and channel forming regions.

[0019]

Since the effect of preventing a depletion layer looks like pinning the depletion layer, the inventors define the term "pinning" as meaning "prevention".

[0020]

[Embodiment Modes of the Invention]

Embodiment modes of the present invention will be hereinafter described in detail by using embodiments to shown below.

[0021]

[Embodiments]

[Embodiment 1]

This embodiment will be described with reference to Fig. 1. Fig. 1 shows a top view, sectional views, and a circuit representation of a non-volatile memory to which the invention is applied. This embodiment is directed to an EEPROM having a basic stacked structure as an example.

[0022]

In Fig. 1, reference numeral 100 denotes a single crystal silicon (p-type silicon); 101, a buried oxide film; 102, field oxide films formed by a LOCOS method; 103, a source region formed by adding arsenic (or phosphorus); and 104, a drain region.

[0023]

Although this is an example structure of an n-type EEPROM in this embodiment, it is also possible to construct a p-type EEPROM. A p-type EEPROM can be constructed by forming source/drain regions by adding boron to an n-type silicon.

[0024]

As the single crystal silicon substrate having a buried oxide film, a SIMOX substrate, a UNIBOND substrate (a substrate adopting a smart cut method), or the like can be used. Naturally, other types of known SOI substrates may also be used.

[0025]

At this time, it is preferable that the thickness of a single crystal silicon thin film formed on the buried oxide film be set to 10 to 100 nm (typically 30 to 50 nm). As the thickness decreases, the hot electron injection occurs more easily and hence the write voltage can be made smaller.

[0026]

Reference numeral 105 denotes impurity regions (hereinafter referred to as pinning regions) that are the most important in the invention. The pinning regions 105 are formed by adding an impurity having the same conductivity type as the silicon substrate 101 (an impurity having a conductivity opposite to the source/drain regions).

[0027]

In this embodiment, since the p-type silicon is used (a single crystal silicon thin film on the buried oxide film is also p-type), they are formed by adding an element selected from group-13 elements (typically boron). Naturally, where an n-type silicon is used (a p-type EEPROM is to be manufactured), pinning regions may be formed by adding an element selected from group-15 elements (phosphorus or arsenic).

[0028]

The element selected from group-13 or group-15 elements shifts the energy band of single crystal silicon and thereby forms an energy barrier to carriers (electrons or holes). In this sense, the pinning regions can also be called energy-banded-shifted regions. Elements other than the group-13 and group-15 elements can also be used as long as they have such an effect.

[0029]

An energy-band-shifting element will be described with reference to conceptual diagrams of Fig. 2. Fig. 2(A) shows an energy band of single crystal silicon. If an impurity element (an element selected from group-13 elements) that shifts the energy band in such a direction as to obstruct the movement of electrons is added there, it is changed to a state as shown in Fig. 2(B).

[0030]

At this time, in the impurity-added region, although no change occurs in the energy band gap, the Fermi level (Ef) is moved to the valence band (Ev) side. As a result, the energy is shifted upward in appearance and hence an energy barrier having higher energy than the undoped regions by ΔE (for electrons) is formed.

[0031]

If an impurity element (an element selected from group-15 elements) that shifts the energy band in such a direction as to obstruct the movement of holes is added, the energy state is

changed as shown in Fig. 2(C).

[0032]

In this case, in the added region, the Fermi level is moved to the conduction band (Ec) side. As a result, the energy is shifted downward in appearance and hence an energy barrier having higher energy than the undoped regions by ΔE (for holes) is formed.

[0033]

As described above, an energy difference of ΔE occurs between the (undoped) regions where the impurity is not added and the pinning regions. The height of the energy (potential) barrier depends on the concentration of the added impurity element. In the invention, the impurity element concentration is adjusted in a range of 1×10^{17} to 5×10^{20} atoms/cm^3 (preferably 1×10^{18} to 5×10^{19} atoms/cm^3).

[0034]

Since the formation of the pinning regions 105 is enabled by microprocessing technology, it is necessary to use an impurity adding method suitable for microprocessing, such as ion implantation or an FIB (focused ion beam) method. Where an adding method using a mask is employed, it is desirable to use microprocessing, such as forming a mask pattern by an electron lithography method.

[0035]

Most typically, the pinning regions 105 are formed in such a manner that the pinning regions 105 and channel forming regions 106 are approximately parallel with each other and are arranged alternately as shown in Fig. 1(A). That is, a structure is preferable in which a plurality of striped pinning regions are provided in a region (active region) enclosed by the source region 103, the drain region 104, and the field oxide films 102.

[0036]

It is effective to form pinning regions at side end portions of the active region (at side end portions where the active region is in contact with the field oxide films). The formation of pinning region at the side end portions can reduce leak current that passes through the side end portions.

[0037]

The pinning regions 105 may be formed so that they at least reach the junction portion of the active region and the drain region 104 (the drain junction portion). Because the depletion layer that causes the punch-through expands from the drain junction portion, an effect can be obtained by preventing this. That is, the expansion of the depletion layer can be suppressed by forming

dot-like or elliptical pinning regions in the active region so that part of them exist in the drain junction portion.

[0038]

Naturally, a more effective pinning effect can be obtained by forming them, from the source region 103 to the drain region 104 as shown in Fig. 1(A).

[0039]

It is desirable that the implantation depth of the pinning regions 105 reach the underlying film 101 or cut into the underlying film 101. In this embodiment, since the thickness of the single crystal thin film is set 10 to 100 nm (typically, 30 to 50 nm), the implantation depth of the pinning regions 105 may be adjusted in a range of 10 to 150 nm (typically, 30 to 100 nm).

[0040]

Now, the channel length and the channel width will be defined with reference to Fig. 3. In Fig. 3, the distance between a source region 301 and a drain region 302 (corresponding to the length of an active region 303) is defined as a channel length (L). The invention is effective in a case where this length L is 2 μm or less, typically 0.05 to 0.5 μm and preferably 0.1 to 0.3 μm. The direction along the channel length is called a channel length direction.

[0041]

The width of an arbitrary pinning region 304 is called a pinning width (v_j). The pinning width may be set to 1 μm or less, typically 0.01 to 0.2μm and preferably 0.05 to 0.1μm. An effective pinning width (V) that is the sum of the widths of all pinning regions existing in the active layer 303 is defined as the following formula.

[0042]

[Formula 1]

[0043]

To obtain the pinning effect, it is necessary to form at least one pinning region in the active region 303; that is, a condition j = 1 or more needs to be satisfied. Where pinning regions are formed at the side end portions (portions adjoining field oxide films) of the active region 303, a condition j = 2 or more needs to be satisfied.

[0044]

The width of a channel forming region 305 is called a channel width (w_i). The channel width can correspond to any case. For memories in which large current is not required, it may be set to 3 μm or less, typically 0.1 to 2 μm, and preferably 0.1 to 0.5 μm.

[0045]

An effective channel width (W) that is the sum of the above channel widths (w_i) is defined as the following formula.

[0046]

[Formula 2]

[0047]

Where the channel width is extremely small, for instance, 0.3 μm or less, the number of pinning regions that can be formed in the active region is limited. In such a case, they may be formed at least only at the side end portions of the active region 303.

[0048]

In such a case, as for the channel width w_i, $i = 1$ is satisfied. To obtain a more effective pinning effect, pinning regions are also preferably formed in regions other than the side end portions of the active region 303. In such a case, i becomes 2 or more.

[0049]

A total channel width W_{total} that is a sum of the sum of the above pinning regions (the effective pinning width) and the sum of the channel forming regions (the effective channel width) is defined as the following formula.

[0050]

[Formula 3]

[0051]

The total channel width (W_{total}) corresponds to the width of the active region 303 (the length of the active region in the direction perpendicular to the channel length direction). The direction along the total channel width is called a channel width direction.

[0052]

Since the invention is intended to be applied to nonvolatile memories having an extremely short channel length as mentioned above, the pinning regions and the channel forming regions need to be formed so as to have extremely small dimensions.

[0053]

In Fig. 1, it is preferable that the impurity element that has been added to the pinning region 105 be activated by furnace annealing, laser annealing, lamp annealing, or the like. The activation process may be performed at the same time as annealing in a later step such as a step of forming a gate insulating film, or independently of it.

[0054]

The invention is characterized in that pinning regions are formed locally (preferably, in striped form) in a region of a conventional nonvolatile memory that serves as a channel forming region. Therefore, the other structures of the conventional nonvolatile memory can be employed as they are.

[0055]

That is, a tunnel oxide film 107 is also formed on the single crystal silicon thin film provided with the source region 103, the drain region 104, and the pinning regions 105. The tunnel oxide film, which is formed by a thermal oxidation step, is required to have high film quality. In this embodiment, the thickness of the tunnel oxide film 107 is set to 11 nm. It goes without saying that the thickness of the tunnel oxide film is not limited to this value.

[0056]

In this embodiment, the pinning regions 105 described above may be formed even after the formation of the tunnel oxide film 107.

[0057]

A first polysilicon layer as a floating gate 108 is formed on the tunnel oxide film 107. It is important to construct so that as shown in Fig. 1(C) the end portions of the floating gate 108 overlap the junction portions of the pinning portions 105 and the drain region 104.

[0058]

A large amount of hot electrons are generated by concentrated electric fields at this junction portions. Therefore, hot electrons can be injected at high efficiency by overlapping the floating gate with this portion.

[0059]

After the formation of the floating gate 108, a first interlayer film 109, a second polysilicon layer as a control gate 110, a second interlayer film 111, and a bit line 112 are formed.

[0060]

Naturally, a conductive layer such as a metal film can be used instead of the polysilicon layer. It is also effective to use, as the interlayer film, a laminated film as expressed by SiO_2/SIN/SiO_2 (commonly called an ONO film).

[0061]

The two-layer polysilicon type EEPROM of this embodiment is given as a circuit diagram shown in Fig. 1(D). In Fig. 1(D), Vd denotes a drain voltage, Vs denotes a source voltage, C.G. denotes a control gate voltage, and F.G. denotes a potential of the floating gate.

[0062]

In the EEPROM of this embodiment, the following voltages are applied at the time of data writing and erasure.

[0063]

[Table 1]

[0064]

Naturally, the operation voltages are not required to be limited to Table 1. Further, the structure of this embodiment is not limited to this, and the invention can be applied to all EEPROMs in which data is erased electrically.

[0065]

(Operation Effect of Embodiment)

A first effect of this embodiment will be described below. In Fig.1, the pinning regions 105 that are locally formed in the active region serve as stoppers with respect to the depletion layer that expands from the drain side and effectively suppress expansion of the depletion layer. Therefore, the punch-through phenomenon that is caused by expansion of the depletion layer can be prevented. Further, since an increase of depletion layer charge due to expansion of the depletion layer is suppressed, a reduction in threshold voltage can be prevented.

[0066]

Next, a second effect will be described. In this embodiment, the narrow channel effect can be enhanced intentionally by the pinning regions. The narrow channel effect, which is a phenomenon observed when the channel width is extremely narrow, causes an increase in threshold voltage (refer to Submicron Devices I, Koyanagi Mitsumasa et al., pp. 88-138, Maruzen Co., Ltd., 1987).

[0067]

Fig. 4 shows an energy state (potential state) of the active region, when the pinning TFT of this embodiment operates. In Fig. 4, regions shown by 401 and 402 represent the energy state of pinning regions 105 and a region shown by 403 represents the energy state of a channel forming region 106.

[0068]

As apparent from Fig. 4, the pinning regions 105 form high-energy barriers and the channel forming regions 106 form low-energy barrier regions. Therefore, carriers move through the channel forming regions 106 with priority where the energy is low.

[0069]

In this manner, high-energy barriers are formed in the pinning regions 105 and the threshold voltage of the part increases. As a result, a threshold voltage that is observed as a whole also increases. This narrow channel effect becomes more remarkable as the effective channel width decreases more.

[0070]

As described above, in the invention, since the concentration of an impurity that is added to the pinning regions 105 and the effective channel width can be designed freely, the threshold voltage can be adjusted by controlling the degree of the narrow channel effect. That is, by controlling the pinning effect, it can be adjusted to a desired value by balancing a threshold voltage decrease due to the short channel effect with a threshold voltage increase due to the narrow channel effect.

[0071]

Since a group-13 element is added to the pinning regions if it is an n-type and a group-15 element is added if it is a p-type, the threshold voltage is shifted in the part in a direction in which the threshold voltage increases (in the positive direction in the case of an n-type and in the negative direction in the case of a p-type). In other words, since the threshold voltage increases locally, the threshold voltage of the entire also increases accordingly. Therefore, to adjust the threshold voltage to a desired value, it is important to set the concentration of an impurity that is added to the pinning regions at a proper value.

[0072]

Incidentally, in nonvolatile memories, discrimination between "0" and "1" is made by changing the threshold voltage by injecting electrons into the floating gate and detecting whether current flows through the bit line when a certain voltage is applied. Therefore, if the threshold voltage is made unduly small by the short channel effect, it becomes necessary to discriminate between "0" and "1" by applying a very small voltage. Namely, it becomes prone to be influenced by noise or the like and the possibility of an erroneous operation increases.

[0073]

However, in the invention, since the threshold voltage can be controlled to have a desired value by suppressing a threshold voltage reduction, the ability of discriminating between "0" and "1" is increased. Therefore, the invention can realize a nonvolatile memory having very high reliability.

[0074]

Next, a third effect will be described. The nonvolatile memory of this embodiment has an advantage that the channel forming regions 106 are made from substantially intrinsic regions, and majority carriers (electrons in the case of an n-type and holes in the case of a p-type) move through the regions.

[0075]

Here, the substantially intrinsic region basically means an undoped single crystal semiconductor region. Besides, it includes a region where conductivity type is offset intentionally by adding an impurity element of the opposite conductivity type, and a region having one conductivity type in a range where the threshold voltage can be controlled.

[0076]

For example, it can be said that a single crystal silicon having a dopant concentration of 5×10^{16} atoms/cm^3 or less (preferably 5×10^{15} atoms/cm^3 or less) and included carbon, nitrogen, and oxygen concentration of 2×10^{18} atoms/cm^3 or less (preferably 5×10^{17} atoms/cm^3 or less) is substantially intrinsic. In this sense, silicon wafers commonly used for ICs are substantially intrinsic unless an impurity is added intentionally in a process.

[0077]

Where a carrier movement region is substantially intrinsic, a mobility reduction due to the impurity scattering is extremely small and hence high carrier mobility is obtained. In other words, the carrier mobility is dominated by the influence of the lattice scattering and is very close to the ideal state.

[0078]

Where the linear pinning regions are formed, from the source region to the drain region as shown in Fig. 1(A), an effect is obtained that movement paths of majority carriers are defined by the pinning regions.

[0079]

As described above, each channel forming region interposed between pinning regions has an energy state as shown in Fig. 4. The structure of Fig. 1(A) is regarded as an arrangement of a plurality of slits having the energy state as in Fig. 4.

[0080]

Fig. 5 schematically illustrates such a state. In Fig. 5, reference numeral 501 denotes pinning regions, and 502; channel forming regions. In addition, 503 denotes majority carriers (electrons or holes). As shown in Fig. 5, the carriers 503 cannot go over the pinning regions

501 and hence move through the channel forming regions 502 with priority. That is, the movement paths of the majority carriers are defined by the pinning regions.

[0081]

Defining the movement paths of majority carriers decreases scattering due to self-collision of carriers, which greatly contributes to mobility increase. Further, since only a very small amount of impurity elements exist in the substantially intrinsic channel forming regions, the velocity overshoot effect occurs, in which the electron mobility becomes higher than usual even at room temperature (refer to K. Ohuchi et al., Jpn. J. Appl. Phys., 35, pp. 960, 1996). Therefore, the mobility becomes extremely high.

[0082]

High carrier mobility that is obtained as described above is effective in shortening the charge write time and the charge read time, thereby increasing the memory performance. High carrier mobility means high energy, and hence the charge writing efficiency is greatly increased by channel hot electron injection (CHE injection).

[0083]

Next, a fourth effect will be described. Where the structure of this embodiment is employed, an electric field is concentrated to a large extent at the junction portions (typically, a p^+/n^{++} junction or an n^+/p^{++} junction is formed) of the pinning regions and the drain region. Therefore, there occur a large amount of electrons that are given high energy through acceleration or generated by impact ionization (collectively called hot electrons).

[0084]

Namely, charge injection into the floating gate is performed very efficiently and hence the data write time can be shortened; specifically, it is reduced to about 1/10 to 1/100 of conventional ones. Therefore, by utilizing the invention, the data write time of a 256 Mbit stacked flash memory, which will be realized in the future, can be made 10 ns/byte or less, preferably 0.01 to 1 ns/byte.

[0085]

Since realization of a data write operation faster than that of magnetic memories is made by this, it becomes possible to replace all kinds of current hard disks that are magnetic memories with flash memories. In other words, since very small chips will have functions equivalent to those of conventional magnetic memories, it is expected that the miniaturization and the price reduction of devices will be accelerated.

[0086]

Moreover, the structure of this embodiment is also effective in decreasing the voltage necessary for data writing (the write voltage). Namely, by virtue of accelerated hot electron injection due to concentrated electric fields at the pinning /drain junction portions, charge of the same amount as in conventional ones can be injected by a write voltage that is 1/2 to 1/10 thereof.

[0087]

Therefore, while current stacked flash memories requires a write voltage of about 10 V, the structure of this embodiment can realize a write voltage of 5 V or less, preferably about 1 to 3 V.

[0088]

As described above, the hot electron injection efficiency at the drain junction portions can be increased by forming the pinning regions. This is effective in reducing the power consumption and increasing the degree of freedom in circuit designing.

[0089]

Next, a fifth effect will be described. The fact that the pinning regions of the invention have the functions of preventing the short channel effect and controlling the threshold voltage has been described above. In addition, it has an important roll in preventing a substrate floating effect due to impact ionization (collisional ionization).

[0090]

Conventionally, electrons of electron-hole pairs generated by impact ionization are injected into the floating gate, and holes are stored under a channel forming region. Diffusion potential on the source side decreases by the influence of the stored holes, and a drain current which does not depend on a control gate is observed (called a substrate floating effect)

[0091]

However, in the invention, holes generated by impact ionization immediately move into the pinning regions and extracted to the source region through the inside thereof. Therefore, the holes are not stored under the channel region and prevention of the substrate floating effect is possible.

[0092]

It goes without saying that this effect is particularly remarkable when the pinning regions are formed, from the source region to drain region. Holes can be extracted more efficiently if the pinning regions are in contact with a pickup electrode in the source region.

[0093]

[Embodiment 2]

The two-layer polysilicon EEPROMs shown in the first embodiment are classified into a byte erasure type (data erasure is performed on a unit memory element basis) and a flash type (data of collective memory elements are erased en bloc).

[0094]

The flash type EEPROM is also called the flash memory. The invention can be applied to either of the two types of EEPROMs.

[0095]

There are various data erasing methods such as a source erasure type, and a source/gate erasure type. The invention can be applied to any of those cases.

[0096]

[Embodiment 3]

While the first and second embodiments have shown the two-layer polysilicon EEPROM, this embodiment describes an example of a case where the invention is applied to a three-layer polysilicon EEPROM with reference to Fig. 6.

[0097]

Since a basic structure is the same as the two-layer polysilicon type EEPROM described in the first embodiment, the reference numerals used for description of Fig. 1 are also used. That is, for the parts shown in Fig. 6 that are given the same reference numerals as in Fig. 1, reference may be made to the descriptions of Fig. 1. In this embodiment, only the different parts will be given new reference numerals and described.

[0098]

Fig. 6(A) is different from Fig. 1(A) in that an erasing gate 701 is provided. That is, a first polysilicon layer constitutes the erasing gate 601 and second and third polysilicon layers constitute the floating gate 108 and the control gate 110, respectively.

[0099]

In the EEPROM that is configured according to the first embodiment, data erasure is performed by extracting, to the source region, electrons that have been injected into the floating gate 108. In contrast, in the structure of this embodiment, data erasure is performed by extracting, to the erasing gate 601, electrons that have been injected into the floating gate 108.

[0100]

Therefore, in Fig. (1)B, an insulating film 602 for insulating and separating the erasing gate

601 and the floating gate 108 should be as thin as possible (preferably 8 to 12 nm) so as to allow a flow of tunnel current (Fowler-Nordheim current) as well as should be of such high quality film as to be highly durable.

[0101]

In the case of this embodiment, it can be manufactured basically by the same process as the structure of the first embodiment with an exception that a step of forming the erasing gate 601 and the erasing gate insulating film 602 after formation of the pinning regions is added.

[0102]

An EEPROM having an erasing gate as in this embodiment is given a circuit diagram shown in Fig. 6(D). In Fig. 6(D), Vd denotes a drain voltage, Vs denotes a source voltage, E.G. denotes an erase gate voltage, C.G. denotes a control gate voltage, and F.G. denotes a floating gate potential.

[0103]

In addition, in the EEPROM of this embodiment, the following voltages are applied at the time of data writing and erasure.

[0104]

[Table 2]

[0105]

Naturally, the operation voltages are not limited to Table 2. Further, the structure of the invention is not limited to this, and the invention can be applied to all types of EEPROMs having an erasing gate structure.

[0106]

[Embodiment 4]

The nonvolatile memories shown in the first to third embodiments utilize hot electron injection for data writing and Fowler-Nordheim current for data erasure. This type of operation mode is often used for a stack type.

[0107]

However, the invention can also be applied to nonvolatile memories using Fowler-Nordheim current also for data writing. This type of operation mode is often used for a NAND type, an AND type, and a DINOR type.

[0108]

In particular, in manufacturing a large-capacity memory of 256 Mbits or more, to improve the reliability (to elongate the life by suppressing deterioration) it is preferable to write data by using

Fowler-Nordheim current.

[0109]

[Embodiment 5]

The first embodiment have described the two-layer polysilicon EEPROM in which data erasure is performed electrically as one example. On the other hand, the nonvolatile memory in which electrons that have been injected into the floating gate are extracted to the source or the substrate by exciting those by ultraviolet illumination or heating is called an EPROM. The invention can also be applied to the EPROM like this.

[0110]

Among EPROMs, there is a nonvolatile memory not using a floating gate in which a two-layer gate insulating film is provided between a control gate and a silicon substrate and hot electrons are captured by interface states thereof. For example, a type in which hot carriers are captured at the interface between a silicon oxide film and a silicon nitride film is called an NMOS nonvolatile memory.

[0111]

Further, there are nonvolatile memories in which hot carriers are captured by metal clusters, silicon clusters, or the like that are formed intentionally at an interface between insulating films.

[0112]

The invention can be applied to all kinds of EPROMs as exemplified above.

[0113]

[Embodiment 6]

The first embodiment has described, as one example, the case (typically a SIMOX substrate) where a buried oxide film is provided in a single crystal silicon and a single crystal silicon thin film is formed thereon. However, a single crystal silicon thin film can be formed on crystallized glass, quartz, or ceramics by utilizing a technique called a smart cut method.

[0114]

Where crystallized glass is used, it is effective to cover the entire surfaces (front, back, and side surfaces) with insulating silicon films. This measure makes it possible to prevent pollution due to glass constituent substances even when a high-temperature heat treatment is performed.

[0115]

Since it is possible to use a crystallized glass having approximately the same thermal expansion coefficient as a silicon film, stress occurring in a silicon thin film can be minimized. This is very important in manufacturing a highly reliable device.

[0116]

For example, in a case of manufacturing a LCD (liquid crystal display) that is constituted of TFTs and nonvolatile memory using a single crystal silicon thin film, no stress-induced warp occurs even if an inexpensive glass substrate is used as an opposed substrate as long as crystallized glass is used as a device-side substrate. (A warp may occur due to a difference in thermal expansion coefficient if quartz used as a device-side substrate, and it is necessary to use an expensive quartz substrate as an opposed substrate.)

[0117]

As described above, constructing a nonvolatile memory in which crystallized glass is used as a substrate and a single crystal silicon thin film is formed on an insulating film that covers it, is very effective in manufacturing a low-price product. The invention can easily be applied to such a case.

[0118]

[Embodiment 7]

Although the first to sixth embodiments have described, as one example, the SOI structure in which a single crystal silicon thin film is used as a semiconductor layer, all the single crystal silicon thin films used in these embodiments may be replaced by polysilicon films.

[0119]

A nonvolatile memory of this embodiment will be described with reference to Fig. 12. Fig. 12(A) is a top view of this embodiment, and Figs. 12(B) and 12(C) are sectional views taken along lines A-A' and B-B' in Fig. 12(A), respectively.

[0120]

In Fig. 12, reference numeral 30 denotes a crystallized glass (glass ceramics). A substrate made of a material having high heat resistance is used because a heat treatment at 700°C or more is needed to form a polysilicon film used in this embodiment.

[0121]

Although quartz may be used as a material having high heat resistance, an inexpensive crystallized glass is used in this embodiment rather than an expensive quartz substrate. In addition, the crystallized glass 30 is covered with a protective film 31 that is made of an insulating silicon film (a silicon oxide film, a silicon nitride film, a silicon oxynitride film, or the like), and thus an escape of glass components is prevented.

[0122]

An active layer that is a polysilicon thin film having a unique crystal structure is formed on

the protective film 31, and a source region 32, a drain region 33, pinning regions 34, and channel forming regions 35 are formed by adding an impurity. A method for forming the polysilicon thin film will be described later.

[0123]

Then, a gate insulating film 36 is formed on the surface of the active layer which is made of polysilicon thin film. Subsequently, an erasing gate 37 and a tunnel oxide film 38 are formed and then a floating gate 39 is formed.

[0124]

Further, a first interlayer film 40 is formed so as to cover the floating gate 39, and a control gate 41, a second interlayer film 42, a ground line 43, and a bit line 44 are sequentially formed to constitute a stacked nonvolatile memory (EEPROM).

[0125]

In this embodiment, as described above, a polysilicon thin film having a unique crystal structure that has been developed by the present applicants is used as the active layer (forming the source region, the channel forming region, and the drain region).

[0126]

Although naturally another polysilicon thin film formed by a known method may be used, to increase the operation speed of the memory itself and decrease the write voltage, it is desirable to use a polysilicon thin film having the above-mentioned unique crystal structure.

[0127]

A technique for forming a polysilicon thin film having this unique crystal structure will be described here with reference to Fig. 13.

[0128]

In Fig. 13(A), reference numerals 50 denotes a crystallized glass and numeral 51 denotes a protective film for preventing an escape of constituent substances from the crystallized glass. An amorphous silicon film 52 is formed thereon by low-pressure CVD, plasma CVD, or sputtering.

[0129]

Where it is formed by low-pressure CVD, it is preferable to remove films formed on the back and side surfaces before a later crystallization step. According to experiences of the inventors, the crystal state appears to be deteriorated if the crystallization step is executed with amorphous silicon films left on the back and side surfaces (the reason is unknown).

[0130]

It is possible to use other semiconductor thin films such as a thin film of a silicon-germanium compound Si_XGe_{1-X} ($0 < X < 1$), in addition to the amorphous silicon film 52. The thickness of the amorphous silicon film 53 may be set to 25 to 100 nm (preferably 30 to 60 nm).

[0131]

Then, the step of crystallizing the amorphous silicon film 52 is executed. As the crystallization means, a technique that is disclosed in Japanese Patent Laid-Open No. Hei. 7-130652 of the present inventors is employed. Although either of the techniques described in the first and second embodiments of this publication may be employed, in this invention it is preferable to use the technique of the second embodiment of this publication (described in more detail in Japanese Patent Laid-Open No. Hei. 8-78329).

[0132]

In the technique disclosed in the publication No. Hei. 8-78329, a mask insulating film 53 for selecting a catalyst element adding region is formed first. A catalyst element containing layer 54 is formed by applying a solution containing a catalyst element for accelerating crystallization of the amorphous silicon film 52 by spin coating (Fig. 13(A)).

[0133]

The catalyst element can be one or a plurality of elements selected from nickel (Ni), cobalt (Co), iron (Fe), palladium (Pd), platinum (Pt), copper (Cu), gold (Au), germanium (Ge), and lead (Pb). It is desirable to use nickel that has a good lattice matching with silicon.

[0134]

The above step of adding the catalyst element may be executed by ion implantation or plasma doping using a mask, without being limited to spin coating. Since this case facilitates reduction of the area occupied by the added region and control of the growth length of a lateral growth region, it is a technique effective in constructing a miniaturized circuit.

[0135]

Next, after the completion of the catalyst element adding step, hydrogen removal is performed at 500°C for about 2 hours. Then, the amorphous silicon film 52 is crystallized by performing a heat treatment at 500°C to 700°C (typically 550°C to 650°C, preferably 570°C) for 4 to 24 hours in an inert atmosphere, a hydrogen atmosphere, or an oxygen atmosphere. (Fig. 13(B))

[0136]

At this time, the crystallization of the amorphous silicon film 52 proceeds with priority from

nuclei that are generated in the region where the catalyst element is added, whereby crystal regions 55 are formed, which has grown approximately parallel with the substrate surface of the crystallized glass 50. The inventors call the crystal regions 55 lateral growth regions. The lateral growth region has an advantage that it has superior crystallinity as a whole because individual crystals are combined together so as to be arranged relatively uniformly.

[0137]

After the completion of the heat treatment for crystallization, the mask insulating film 53 is removed. Then, a heat treatment for removing the catalyst element (catalyst element gettering step) is performed. In this heat treatment, a halogen element is mixed into a processing atmosphere to utilize the metal element gettering effect of the halogen element.

[0138]

To fully effectuate the gettering effect of the halogen element, it is preferable to perform the heat treatment at a temperature higher than 700°C. At a temperature equal to or lower than this temperature, there is a possibility that a halogen compound in the processing atmosphere is hard to decompose and resultantly the gettering effect is not obtained. It is preferable to set the heat treatment temperature at 800 to 1,000°C (typically 950°C) and time 0.1 to 6 hours, typically 0.5 to 1 hour.

[0139]

Typically, the heat treatment may be performed at 950°C for 30 minutes in an oxygen atmosphere containing a hydrogen chloride (HCl) gas at 0.5 to 10 vol% (preferably 3 vol%). A HCl density higher than the above density is not preferable because asperities whose heights are on the order of the film thickness will occur on the silicon surface.

[0140]

Other than HCl, the compound containing a halogen element may be one or a plurality of compounds containing a halogen element selected from HF, NF_3, HBr, Cl_2, ClF_3, BCl_3, F_2, and Br_2.

[0141]

In this step, the catalyst element in the lateral growth regions 55 is gettered by the action of chlorine and withdrawn and removed into the air in the form of a volatile chloride. After this step, the concentration of the catalyst element in lateral growth regions 56 is reduced to 5×10^{17} atoms/cm^3 or less (typically 2×10^{17} atoms/cm^3 or less).

[0142]

Although in this embodiment the catalyst element is gettered by the gettering ability of a

halogen element, it is also possible to utilize the gettering ability of the element of phosphorus. In gettering is conducted by using phosphorus, a layer containing phosphorus at a high concentration may be provided adjacent to the lateral growth regions and a heat treatment may be performed to cause the phosphorus-containing layer to getter the catalyst element.

[0143]

The resulting lateral growth regions 56 has a unique crystal structure that is a collected body of rod-like or flat-rod-like crystals. In the nonvolatile memory of this embodiment, a polysilicon thin film constituted of only a lateral growth region 56 is used as the active layer.

[0144]

Specifically, the unique crystal structure is a structure in which rod-like crystals are arranged approximately parallel with each other and have particular directivity macroscopically. Further, individual rod-like crystals are connected to each other with extremely high continuity at their grain boundaries.

[0145]

Detailed observation results of such a state are described in Japanese Patent Application Serial Nos. Hei. 9-55633, Hei. 9-165216, and Hei. 9-212428.

[0146]

A polysilicon thin film formed by the above steps has grain boundaries where crystals are connected to each other with extremely high continuity (with a high level of matching), and they cause almost no obstruction to carrier movements. That is, it can be regarded as a silicon thin film having substantially no grain boundaries and hence can substantially be regarded as a single crystal (as a matter of fact, an electron beam diffraction pattern is very close to a diffraction pattern of a single crystal).

[0147]

Further, the above polysilicon thin film is intrinsic or substantially intrinsic unless no impurity is added intentionally. The term intrinsic as used here means a state that impurities other than silicon are eliminated as much as possible and the polarity is almost negligible.

[0148]

The invention can be applied to all kinds of nonvolatile memories using a semiconductor thin film that can substantially be regarded as a single crystal (a polycrystalline semiconductor thin film having the crystal structure described in this embodiment).

[0149]

[Embodiment 7]

This embodiment will describe a case where an impurity element for imparting the same conductivity type as that of the pinning regions is added to the insulating layer (buried oxide film or the like) that underlies the semiconductor layer in the nonvolatile memory of the first to sixth embodiments.

[0150]

In this embodiment, boron is used as an impurity that is added to the pinning regions. Figs. 14(A) and 14(B) are sectional views that are focused on a channel forming region of a nonvolatile memory according to this embodiment. That is, Figs. 14(A) and 14(B) are sectional views taken along the channel width direction of a channel forming region.

[0151]

In Fig. 14(A), reference numeral 61 denotes a single crystal silicon substrate; 62, a buried oxide film; 63, a channel forming region; and 64 and 65, pinning regions. This embodiment is characterized in that a boron-added region 67 is provided in the buried oxide film 62 in the vicinity of its surface.

[0152]

The structure of Fig. 14(B) is the same as that of Fig. 14(A), but boron is added to the entire buried oxide film 62.

[0153]

Fig. 14(C) schematically shows an energy state of the channel forming region having the structure shown in Fig. 14(A). In Fig. 14(C), 68 is a region in which the energy barrier is low and it serves as a channel forming region.

[0154]

High-energy barrier regions 69 due to leakage of the impurity element are formed in the vicinity of the pinning regions 64 and 65 and the buried oxide film 62 to which boron has been added intentionally.

[0155]

Figs. 14(D) and 14(E) show energy distribution of the channel forming region. That is, Fig. 14(D) is an energy distribution chart taken along a dotted line X in Fig. 14(C) and the horizontal axis represents the distance in the channel width direction and the vertical axis represents the relative energy. Fig. 14(E) is an energy distribution chart taken along a dotted line Y in Fig. 14(C) and the horizontal axis represents the relative energy and the vertical axis represents the distance in the depth direction.

[0156]

The energy distribution charts of Figs. 14(D) and 14(E) are so drawn as to correspond to the energy state chart of Fig. 14(C).

[0157]

As shown in Fig. 14(D), the large relative energy corresponding to **b** is shown in the pinning regions and their vicinities. However, in the inside (in particular, a portion farthest from the pinning regions) of a carrier movement region 68, the relative energy has the minimum value (corresponding to **a**).

[0158]

In addition, as shown in Fig. 14(E), the energy distribution taken along the dotted line Y is such that the relative energy is relatively high in the vicinity of the gate insulating film (not shown) and has the minimum value **a** in the inside of the carrier movement region 68. The relative energy gradually increases as it approaches the interface with the buried oxide film 62 and reaches a value **b'**.

[0159]

If the concentration of the impurity added to the pinning regions and that of the impurity added to the buried oxide film are the same, **b** is equal to **b'**. If they are different adding concentration, **b** is not equal to **b'**. The invention may be of either case.

[0160]

In the invention, it is preferable that the relative energy value (**b** or **b'**) be three times or more (ever preferably 10 times or more) larger than the relative energy value (**a**). This provides a structure in which carriers (electrons or holes) move through the low-energy state region 68 with priority.

[0161]

Since a high energy barrier is formed at the interfaces between the channel forming region 63 and the buried oxide film 62 and its vicinity and keeps carriers away from itself, carrier scattering can be prevented from occurring in the vicinity of the surface of the underlying film (buried oxide film).

[0162]

The above structure makes it possible to effectively suppress expansion of the depletion layer and to further increase the resistance to the short channel effect. In addition, by reducing carrier scattering in the surface of the underlying film, the hot electron injection can be made more efficient.

[0163]

[Embodiment 8]

The nonvolatile memories shown in the first to seventh embodiment can be applied to all the known circuit configurations using nonvolatile memories. This embodiment will describe a case where the invention is applied to flash memories that are designed according to the NAND and NOR type architectures.

[0164]

First, a description will be made of the configuration of a NAND-type memory circuit shown in Figs. 7(A) and 7(B). In Fig. 7, two circuits composed of eight memory transistors and two selection transistors are shown; however, the description only regarding the one thereof is made.

[0165]

As shown in Fig. 7(A), reference numerals 701 and 702 denote selection transistors, and have selection lines S1 and S2 denoted by 703 and 704 as gate electrodes, respectively. The selection transistor 701 connects a bit line 705 shown by B1 (or B2) to eight memory transistors 706 to 713.

[0166]

Although this embodiment shows an example of a case where eight memory transistors are connected in series, it is not limited to this number.

[0167]

The selection transistor 702 is connected to a final-stage memory transistor 713. The other terminal of the selection transistor 702 is grounded. Even if it is connected to a power supply line without being grounded, it can still operate.

[0168]

The memory transistors 706 to 713 use word lines 714 to 721 (shown by W1-W8) as control gates, respectively.

[0169]

Fig. 7(B) is a schematic circuit pattern of the NAND-type memory circuit of Fig. 7(A). In the respective memory transistors, hatched regions are floating gates that are provided under the control gates 714 to 721.

[0170]

Next, a description will be made of the configuration of a NOR-type memory circuit shown in Figs. 8(A) and 8(B). In addition, in Fig. 8, two circuits composed of four memory transistors are shown; however, the description only regarding the one thereof is made.

[0171]

As shown in Fig. 8(A), four memory transistors 802 to 805 are individually connected to a bit line 801 shown by B1. Those terminals (source regions) of the memory transistors 802 to 805 which are not connected to the bit line 801 are connected to a ground line 806.

[0172]

The memory transistors 802 to 805 use word lines 807 to 810 shown by W1-W4 as control gates, respectively.

[0173]

Fig. 8(B) shows schematic circuit pattern of the NOR-type memory circuit of Fig. 8(A). In the respective memory transistors, hatched regions are floating gates that are provided under the control gates 807 to 810, respectively.

[0174]

Although NAND-type circuits as shown in Fig. 7 have disadvantages that the order of writing is fixed and the read access time is slow, they have an advantage that the integration degree can greatly be increased.

[0175]

The configuration of the NOR-type circuit shown in Fig. 8 is effective in injecting electrons precisely into the floating gates and reading out charge amounts precisely. This is the feature of the NOR architecture in which individual memory transistors are directly connected to a source/drain bus line.

[0176]

Although this embodiment is directed to the nonvolatile memory using a two-layer electrode structure (polysilicon or the like), the same nonvolatile memory can be configured by using the three-layer electrode structure (including the erasing gate) as described above in the third embodiment.

[0177]

[Embodiment 9]

This embodiment describes an example of a case where a nonvolatile memory according to the invention is applied to a microprocessor such as a RISC processor or an ASIC processor that is integrated on one chip.

[0178]

Fig. 9 shows an example of a microprocessor, which is typically composed of a CPU core 11, a flash memory 12 (or a RAM), a clock controller 13, a cache memory 14, a cache controller 15,

a serial interface 16, an I/O port 17, and the like.

[0179]

The microprocessor of Fig. 9 is a simplified example. Naturally, a variety of circuit designs are employed in actual microprocessors in accordance with their uses.

[0180]

In the microprocessor of Fig. 9, the CPU core 11, the clock controller 13, the cache controller 15, the serial interface 16, and the I/O port 17 are constituted of CMOS circuits 18. Pinning regions 19 disclosed in the invention are formed in the CMOS circuits 18.

[0181]

In this manner, the invention can be applied to SOIFETs as well as nonvolatile memories. The detail thereof has already been filed with Japanese Patent Application No. Hei.8-239215.

[0182]

The flash memory 14 uses nonvolatile memory according to the invention that form a memory circuit 20. Every memory cell that constitutes the memory circuit 20 is formed with pinning regions 21. It is possible to use nonvolatile memory according to the invention also in the cache memory 12.

[0183]

As described above, in the example of Fig. 9, the pinning technology of the invention is utilized in all of the memory sections and the logic sections.

[0184]

Further, as occasion demands, a configuration shown in Fig. 10 can be employed. Fig. 10 shows an example of a case where the logic sections excluding the memory sections are formed by ordinary CMOS circuits 22. In this case, a configuration may be employed, in which forming pinning regions are not formed only in the logic sections.

[0185]

In this manner, it is possible to form pinning regions, at the circuit designing stage, in necessary sections; a party who practices may determine at will whether to form pinning regions in the entire circuit or only part of it. Where the invention is applied to a hybrid IC in which various functions are combined, such a degree of freedom in circuit design is very effective.

[0186]

[Embodiment 10]

A semiconductor circuit (memory circuit) formed by nonvolatile memories according to the invention can be incorporated, as a recording medium for data storage and readout, in electronic

apparatuses of every field. In this embodiment, examples of those electronic apparatuses will be shown in Fig. 11.

[0187]

As electronic apparatuses which can use a nonvolatile memory of the invention, a video camera, an electronic still camera, a projector, a head-mounted display, a car navigation apparatus, a personal computer, portable information terminals (a mobile computer, a cellular telephone, a PHS, etc.) are given.

[0188]

Fig. 11(A) shows a cellular telephone, which is composed of a main body 2001, a voice output section 2002, a voice input section 2003, a display device 2004, manipulation switches 2005, and an antenna 2006. The invention is incorporated in a built-in LSI board and used to add an address function for recording telephone numbers, etc.

[0189]

Fig. 11(B) shows a video camera, which is composed of a main body 2101, a display device 2102, a sound input section 2103, manipulation switches 2104, a battery 2105, and an image receiving section 2106. The invention is incorporated in a built-in LSI board and used for such a function as storage of image data.

[0190]

Fig. 11(C) shows a mobile computer (mobile computer), which is composed of a main body 2201, a camera section 2202, an image receiving section 2203, a manipulation switch 2204, and a display device 2205. The invention is incorporated in a built-in LSI board and used for storage of processed data and image data.

[0191]

Fig. 11(D) shows a head-mounted display, which is composed of a main body 2301, display devices 2302, and a band section 2303. The invention is used as an image signal correction circuit and is connected to the display devices 2302.

[0192]

Fig. 11(E) shows a rear type projector, which is composed of a main body 2401, a light source 2302, a display device 2403, a polarizing beam splitter 2404, reflectors 2405 and 2406, and a screen 2407. The invention can be used as a storage circuit for storing data to be supplied to a γ-correction circuit.

[0193]

Fig. 11(F) shows a front type projector, which is composed of a main body 2501, a light

source 2502, a display device 2503, an optical system 2504, and a screen 2505. The invention can be used as a storage circuit for storing data to be supplied to a γ-correction circuit.

[0194]

As described above, the application range of the invention is extremely wide and can be applied to electronic apparatuses of every field. In addition to these, it can be used as a storage medium that is indispensable in various control circuits and information processing circuits.

[0195]

[Effect of the Invention]

The invention makes it possible to minimize influences of the miniaturization effects as typified by the short channel effect and to further advance the miniaturization of nonvolatile memories.

[0196]

Small-area, large-capacity nonvolatile memories can be realized while securing their high reliability.

[Brief Description of the Drawings]

[Fig. 1] A view showing the structure of a nonvolatile memory of the present invention.

[Fig. 2] A view illustrating changes of an energy band.

[Fig. 3] A view illustrating definitions of a channel length and a channel width.

[Fig. 4] A view illustrating an energy state in an active region.

[Fig. 5] A view illustrating an energy state in an active region.

[Fig. 6] A view showing the structure of a nonvolatile memory of the invention.

[Fig. 7] A view showing a circuit using a nonvolatile memory of the invention.

[Fig. 8] A view showing a circuit using a nonvolatile memory of the invention.

[Fig. 9] A view showing a semiconductor circuit using a nonvolatile memory of the invention.

[Fig. 10] A view showing a semiconductor circuit using a nonvolatile memory of the invention.

[Fig. 11] A view showing an electronic apparatus using a nonvolatile memory of the invention;

[Fig. 12] A view showing the structure of a nonvolatile memory of the invention.

[Fig. 13] A view showing a manufacturing process of a polysilicon thin film.

[Fig 14] A view showing an energy distribution in a vicinity of a channel forming region.

[Name of Document] ABSTRACT

[Abstract]

[Object] A high-performance memory is realized by effectively preventing the short channel effect that occurs in miniaturizing nonvolatile memories.

[Means for solving] In a nonvolatile memory, in an active region surrounded by a field oxide film 102, a source region 103 and a drain region 104, a pinning region 105 is formed locally. In the invention, a depletion layer expanding from a drain side toward a source side is suppressed by the pinning region 105, and a punch-through phenomenon due to a short channel effect is prevented.

[Selected drawing] Fig. 1

Reference No. P003782-01
Document where chemical formulas etc. are descibed
Name of Document Specification

[Formula 1]

$$V = \sum_{j=1}^{n} v_j$$

[Formula 2]

$$W = \sum_{i=1}^{m} w_i$$

[Formula 3]

$$W_{total} = V + W$$

Reference No. P003782-01
Document where chemical formulas etc. are descibed
Name of Document Specification

[Table 1]

mode	Vd	V_{CG}	Vs	mechanism
at writing	6	12	0	hot electron injection
at erasing	-	0	12	F-N tunnel erasure
at readout	~1	5	0	-

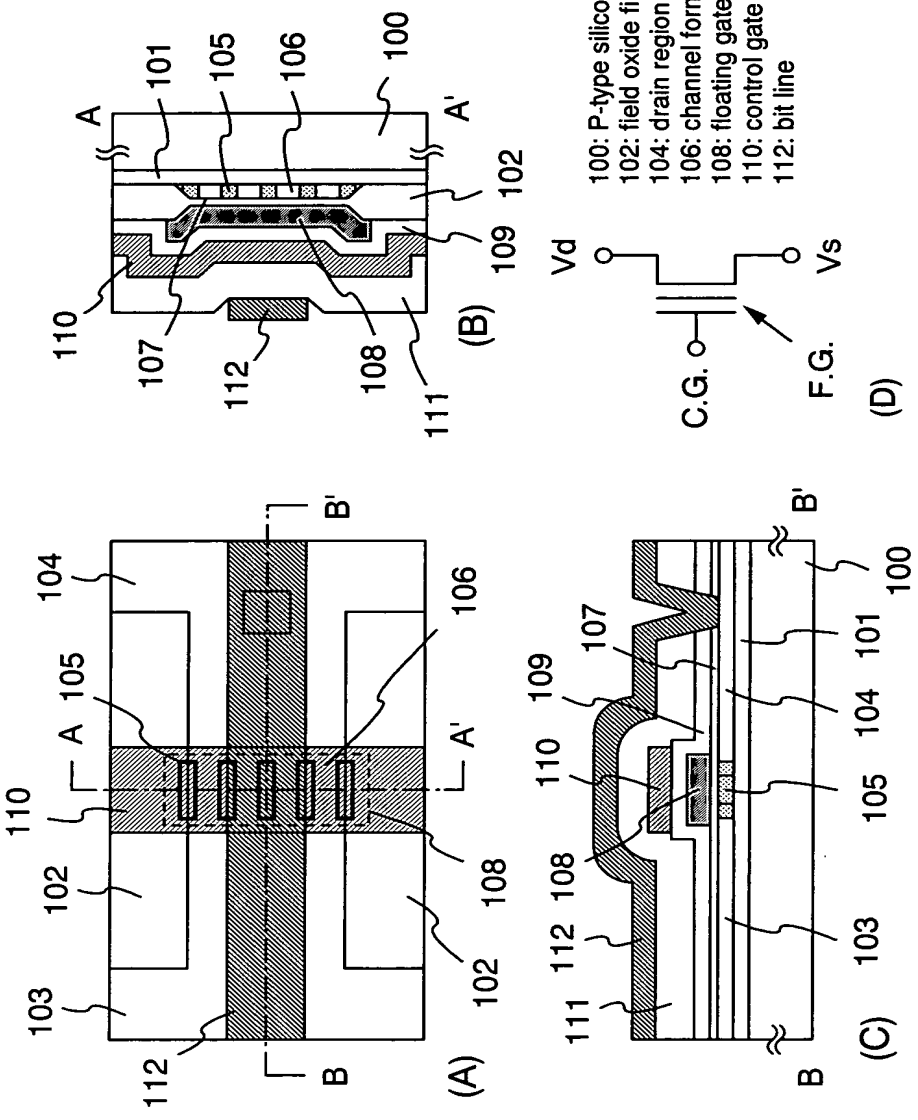
[Table 2]

mode	Vd	Vs	V_{EG}	V_{CG}	mechanism
at writing	8	0	3	12	hot electron injection for floating gate
at erasing	-	0	20	0	F-N tunnel erasure from floating gate
at readout	1	0	0	5	-

[Reference No.] P003782-01

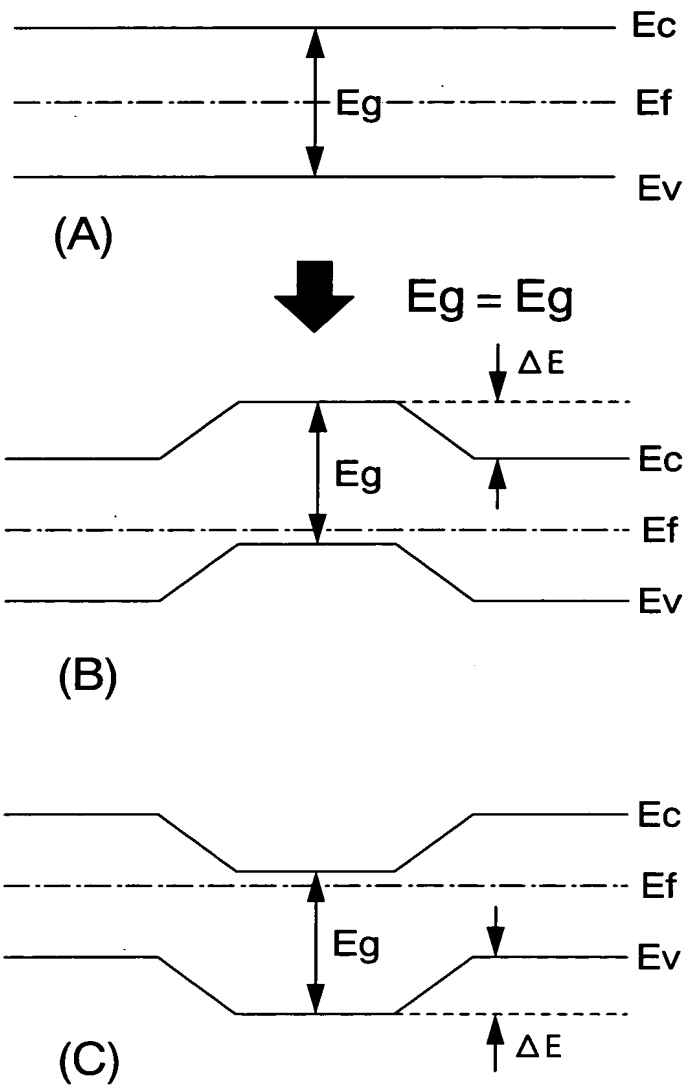
[Name of Document] Drawing

[Fig. 1]



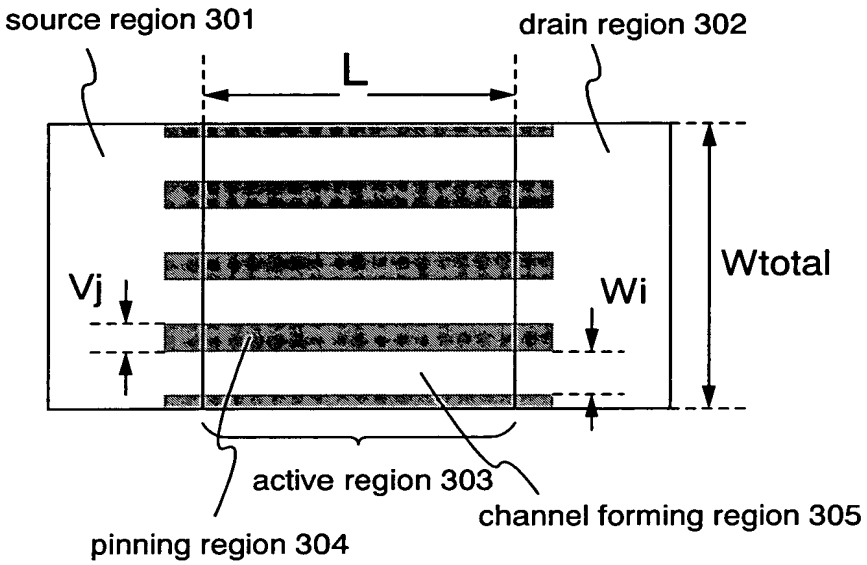
[Reference No.] P003782-01

[Fig. 2]

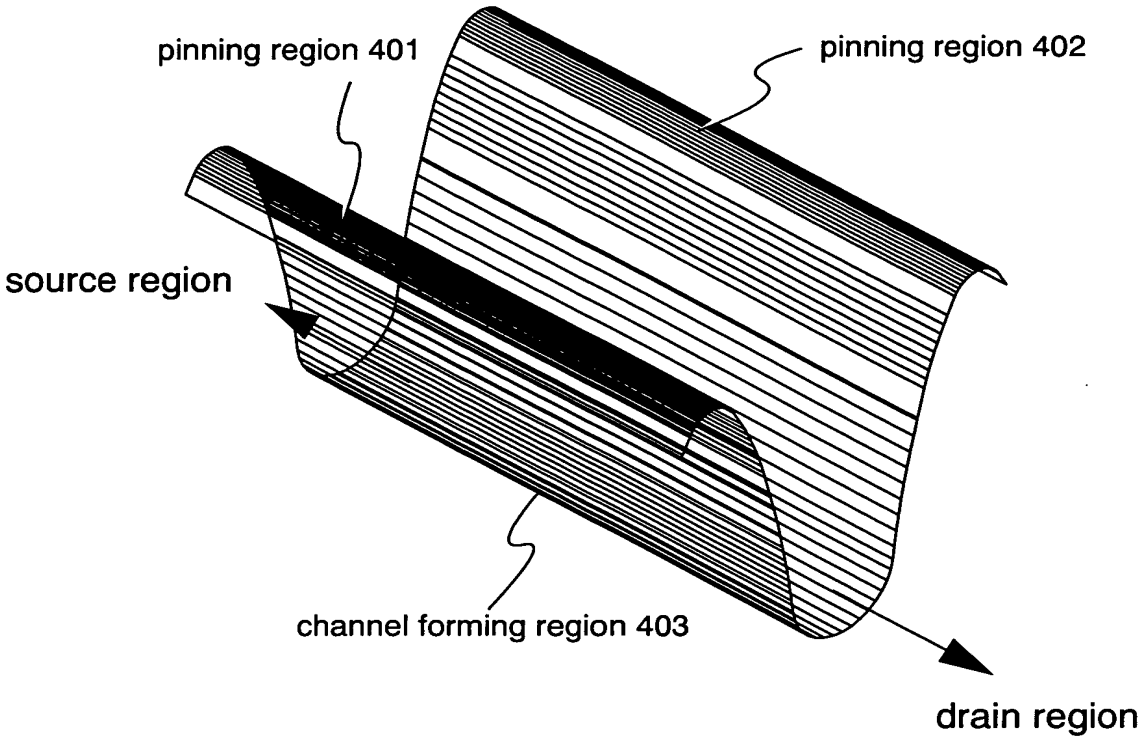


[Reference No.] P003782-01

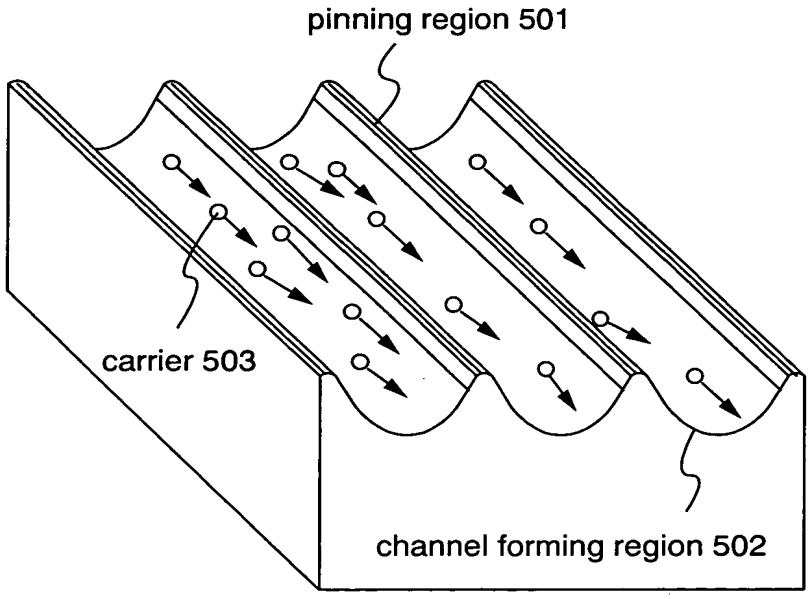
[Fig. 3]



[Fig. 4]

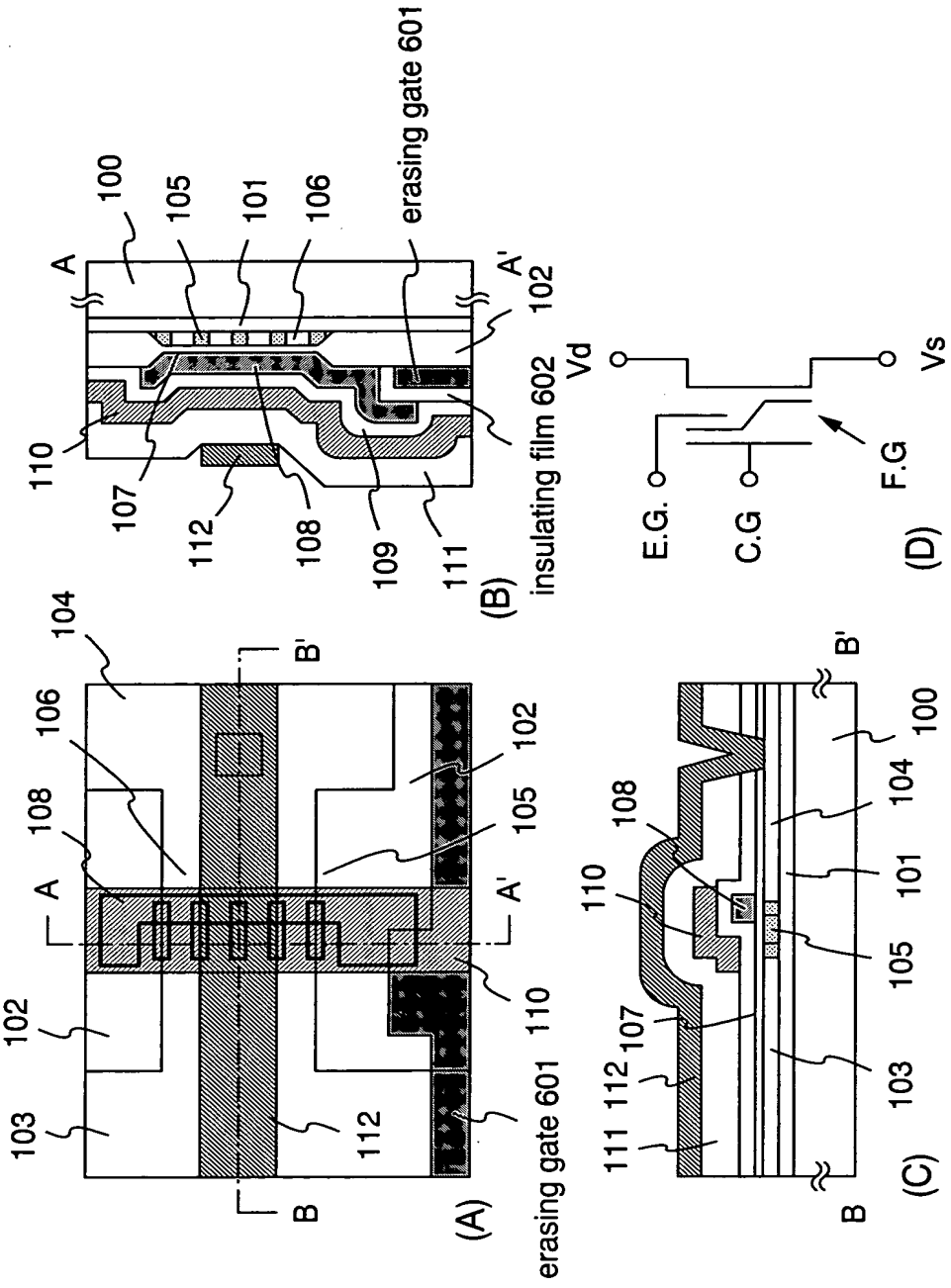

pinning region 401
pinning region 402
source region
channel forming region 403
drain region

[Fig. 5]


pinning region 501
carrier 503
channel forming region 502

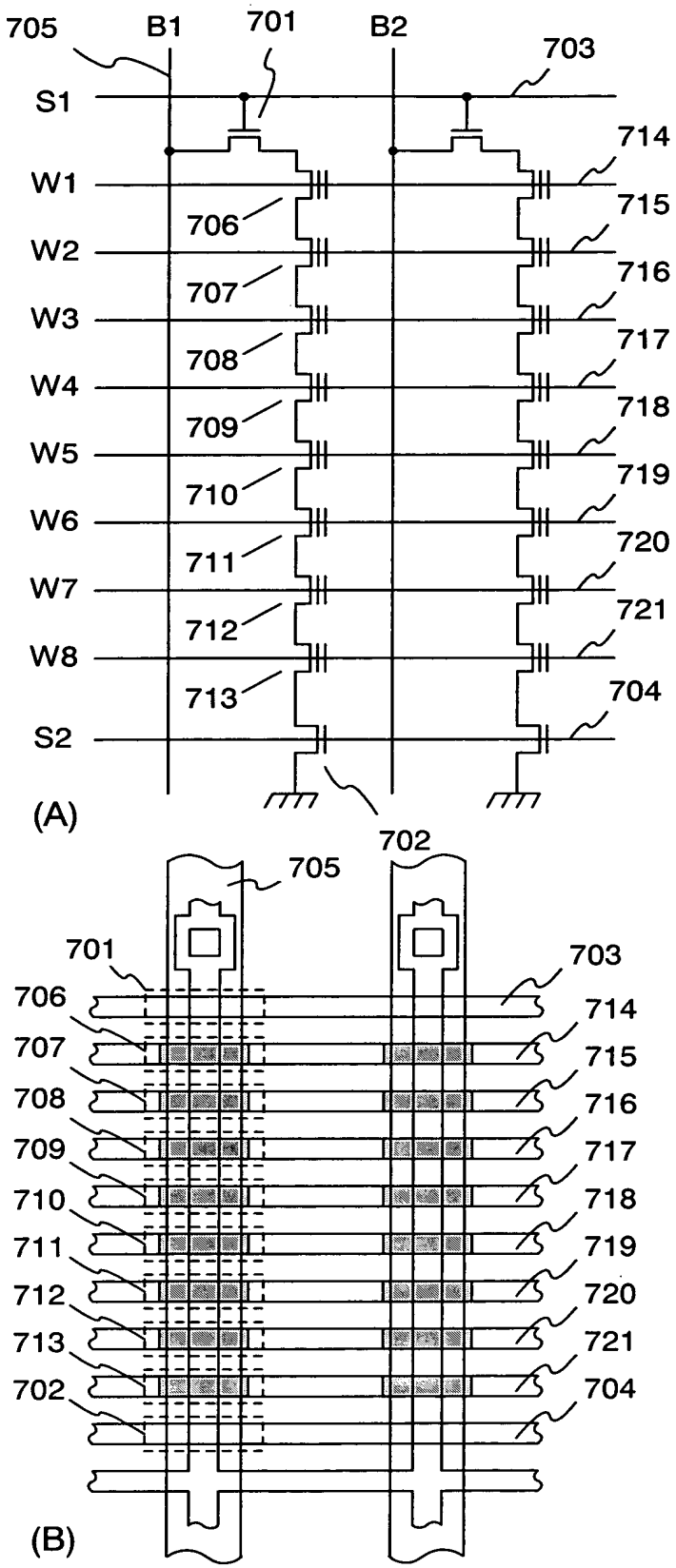
[Reference No.] P003782-01

[Fig. 6]

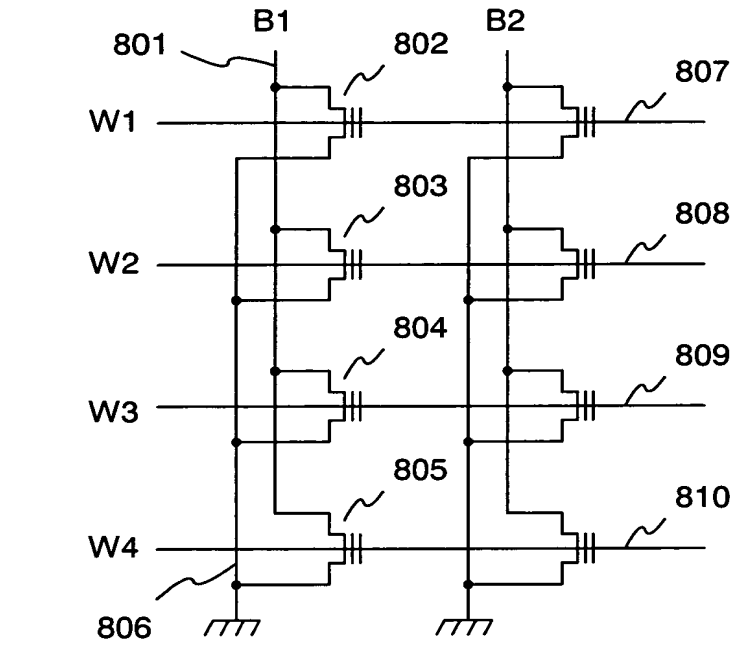


[Reference No.] P003782-01

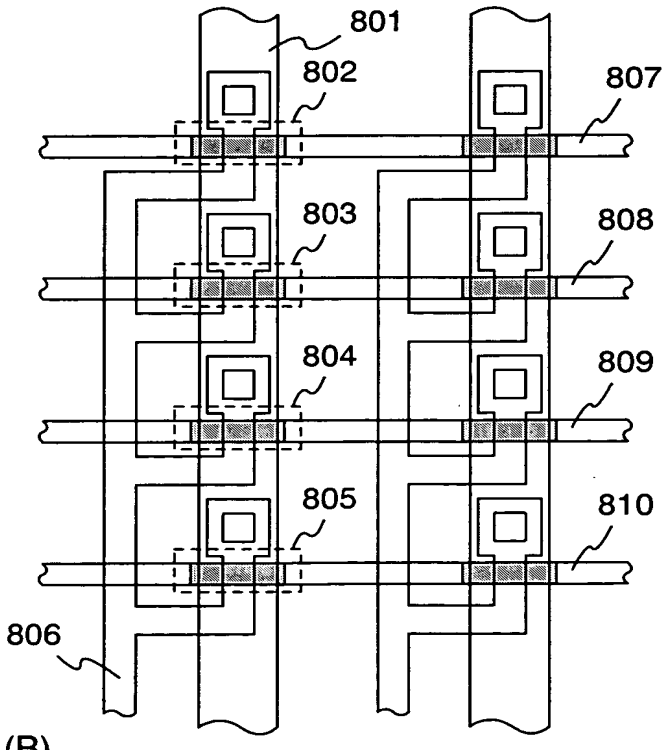
[Fig. 7]



[Reference No.] P003782-01
[Fig. 8]

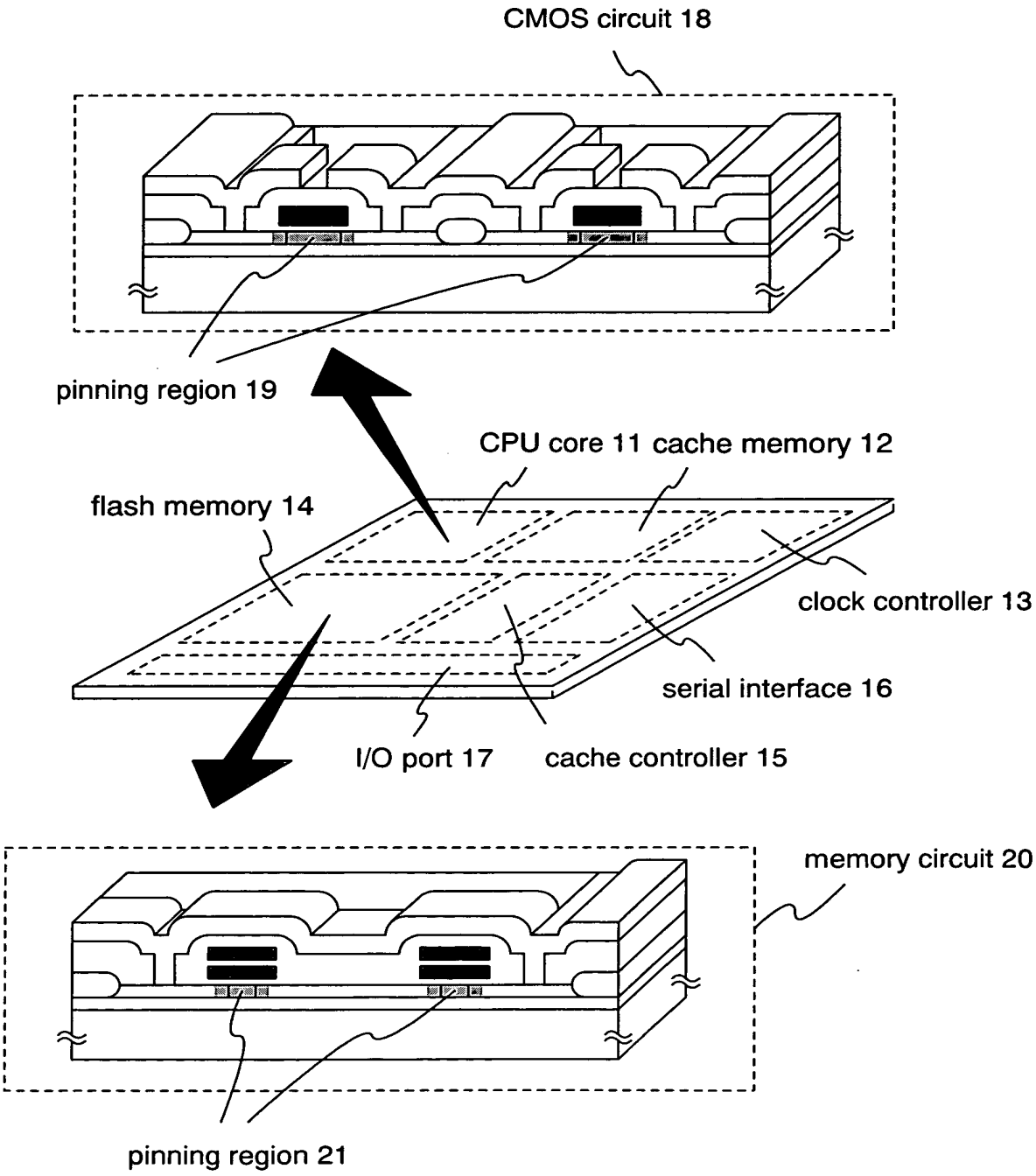


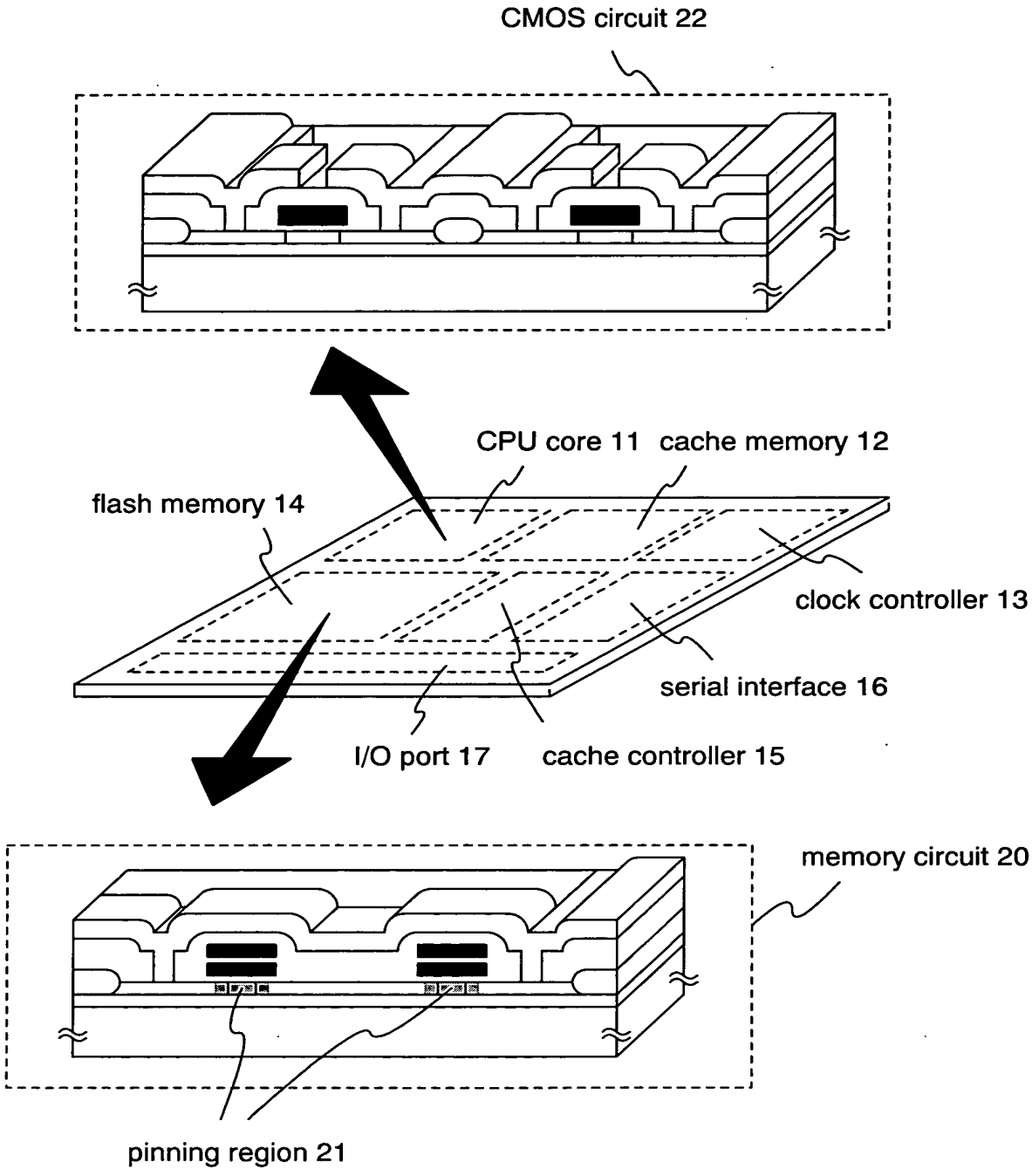
(A)

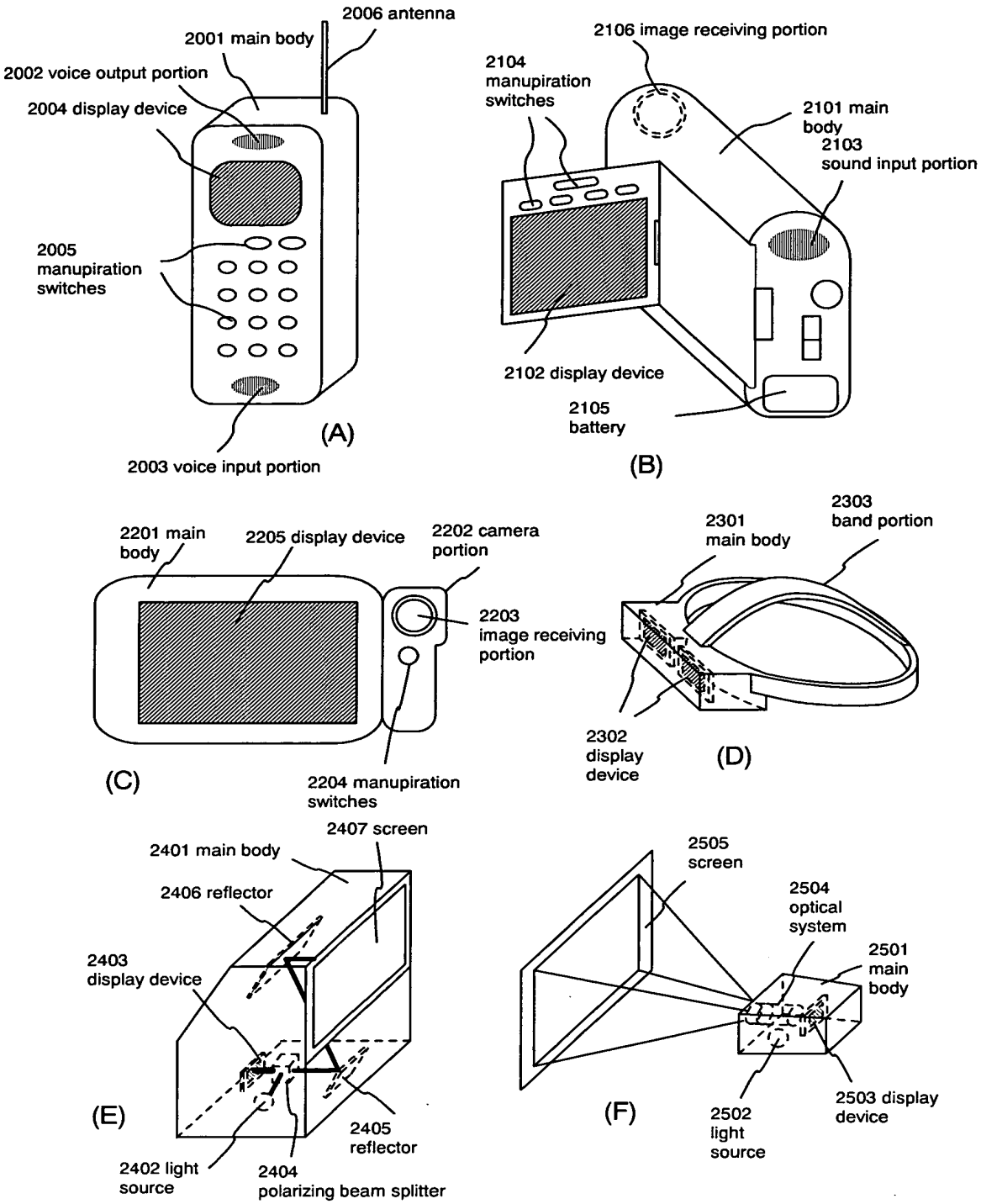


(B)

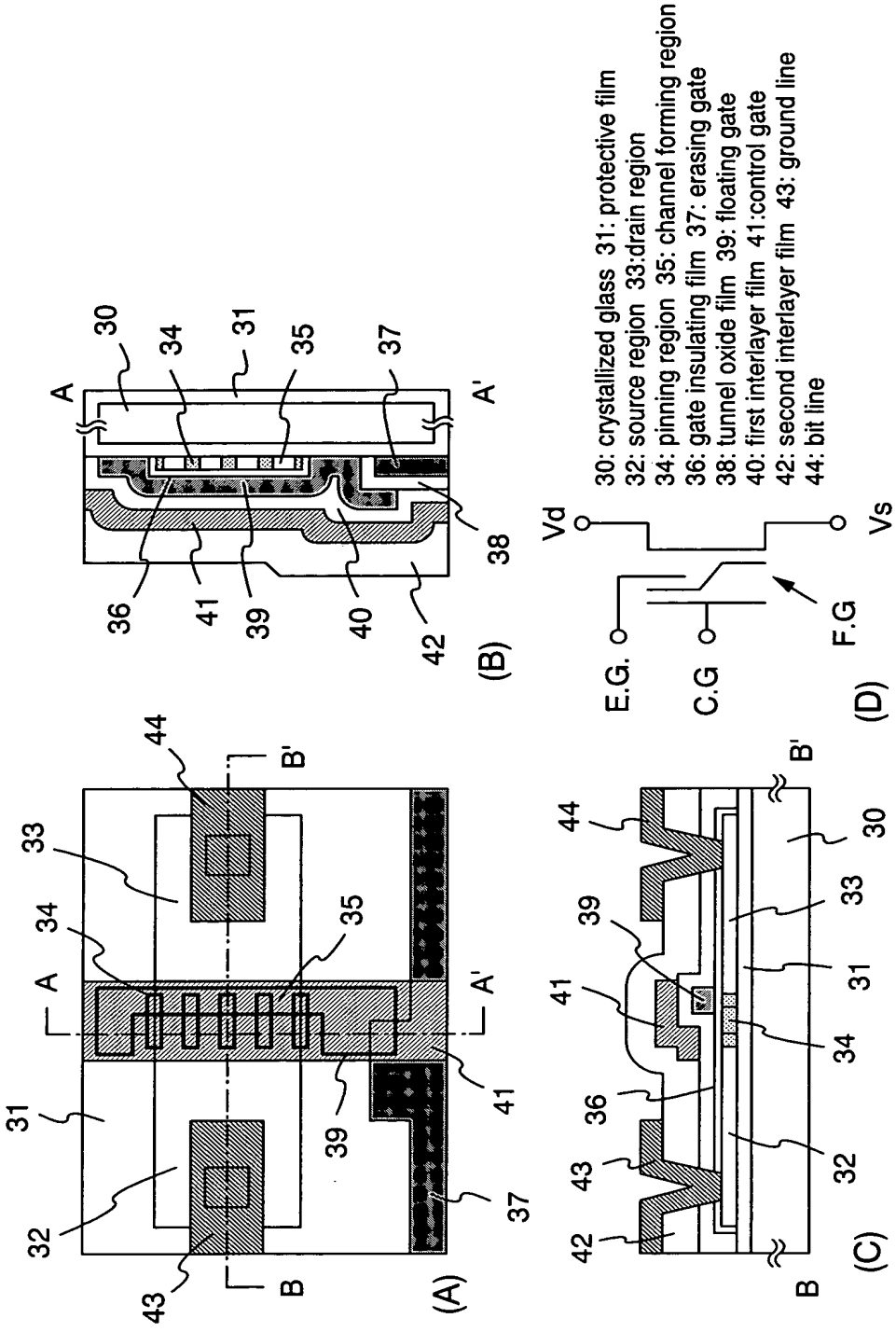
[Reference No.] P003782-01
[Fig. 9]




CMOS circuit 22
CPU core 11
cache memory 12
flash memory 14
clock controller 13
serial interface 16
I/O port 17
cache controller 15
memory circuit 20
pinning region 21

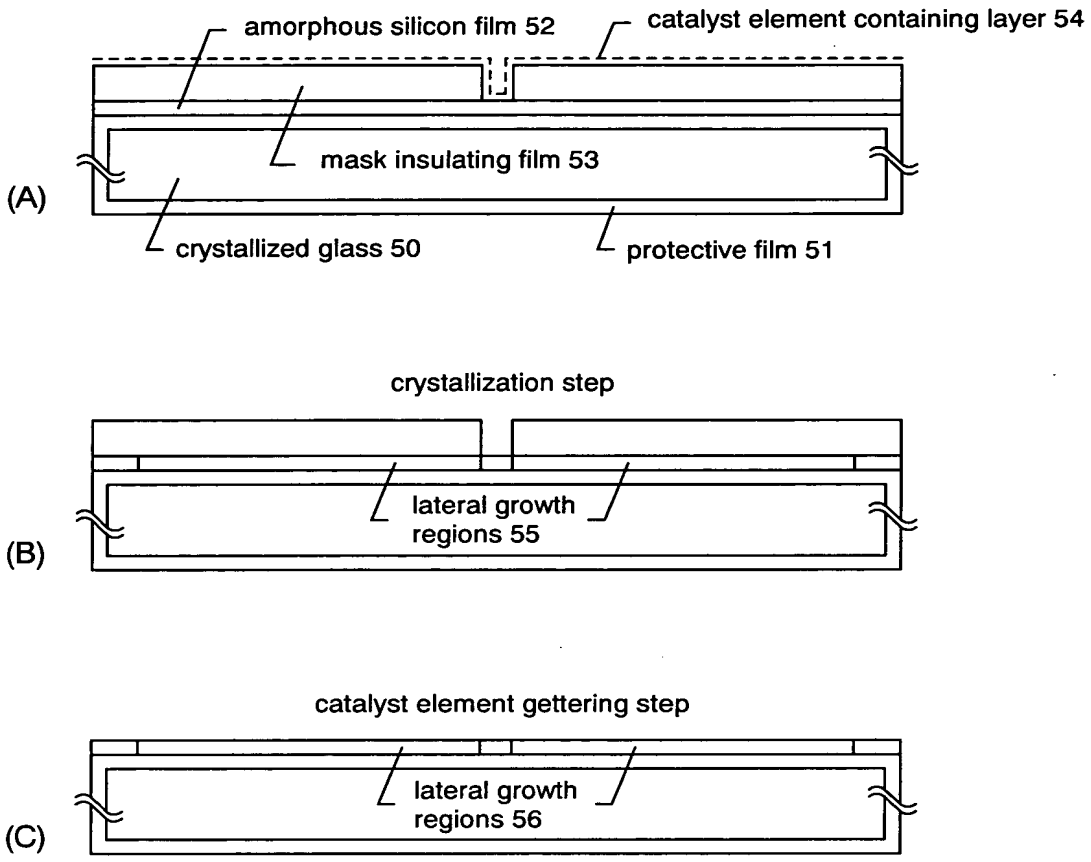

2006 antenna
2001 main body
2002 voice output portion
2004 display device
2005
manupiration
switches
2003 voice input portion
(A)
2106 image receiving portion
2104
manupiration
switches
2101 main
body
2103
sound input portion
2102 display device
2105
battery
(B)
2201 main
body
2205 display device
2202 camera
portion
2203
image receiving
portion
2204 manupiration
switches
(C)
2303
band portion
2301
main body
2302
display
device
(D)
2407 screen
2401 main body
2406 reflector
2403
display device
2405
reflector
2402 light
source
2404
polarizing beam splitter
(E)
2505
screen
2504
optical
system
2501
main
body
2503 display
device
2502
light
source
(F)

[Reference No.] P003782-01
[Fig. 12]

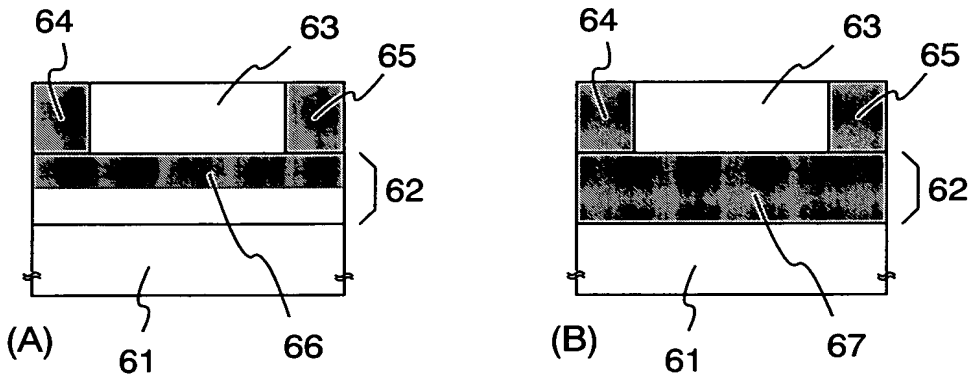


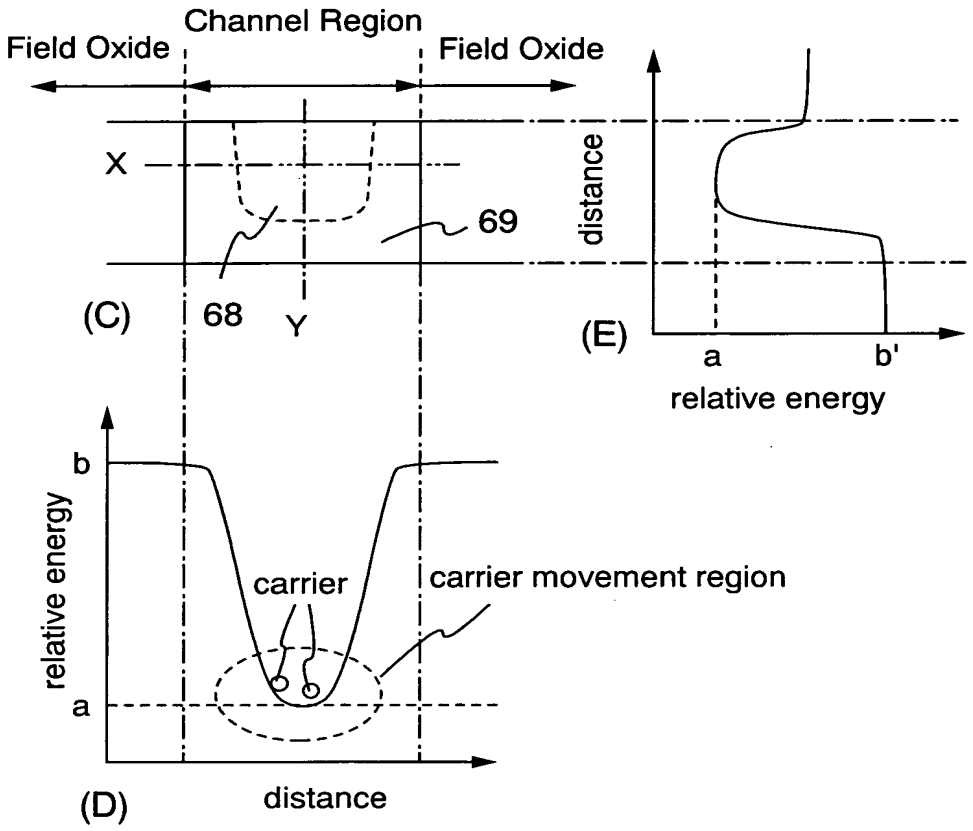
[Reference No.] P003782-01

[Fig. 13]



[Fig. 14]


64
63
65
62
(A)
61
66
64
63
65
62
(B)
61
67


Field Oxide
Channel Region
Field Oxide
X
69
(C)
68
Y
distance
(E)
a
b'
relative energy
b
relative energy
carrier
carrier movement region
a
(D)
distance